PWB/FPC FABRICATION SPECIFICATION

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A	Initial Release	05-26-23
B	Updated: vias negative tolerance to nominal, relaxed requirements for microvias to IPC class 3, ENIG/ENEPIG plating to corresponding IPC specifications, wording clarification on solderability testing, wording clarification on coupons requirements, prepacking boards bakeout temperature range.	09-26-23

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CONTENTS

1.0 PURPOSE AND SCOPE 3
2.0 REFERENCED STANDARDS AND SPECIFICATIONS 3
3.0 TERMS, ACRONYMS AND DEFINITIONS 4
4.0 QUALIFICATION 4
4.1 Determination of Manufacture Qualifications 5
4.2 Qualification of Special Features 5
5.0 RESOLUTION OF CONFLICTING REQUIREMENTS 5
6.0 DEVIATIONS 5
7.0 PWB/FPC FABRICATION 6
7.1 Materials 6
7.1.1 Laminate 6
7.1.2 Metallic Foil 7
7.1.3 Constraining and Heatsinking Cores 8
7.1.4 Solder Mask 8
7.2 PWB/FPC Thickness 10
7.3 Dielectric Separation 10
7.4 Conductors 10
7.5 Hole Tolerances and Registration 12
7.5.1 Annular Ring 13
7.6 Drilling 13
7.6.1 Etchback * 13
7.7 Copper Plating 15
7.7.1 Copper Voids in Holes 15
7.8 Via Plugging and Capping * 15
7.9 Rigid-Flex Strain Relief 15
7.10 HDI (High Density Interconnects) 16
7.10.1 Requirements for µVias Target Lands Contact 16
7.11 Final External Finishes 16
7.12 Silk Screen 17
7.13 Markings 17
7.13.1 Required Markings 18
7.14 Panelization 18
7.15 Repairs 18
7.16 Electrical Testing 18
7.17 Finished Properties 19
7.17.1 Solderability and Structural Integrity 19
7.17.2 Edges of the Board 19
7.17.3 Bow and Twist 19
8.0 CONFORMANCE AND ACCEPTANCE 19
8.1 Microsection Evaluations 19
8.2 Evaluation Coupons and Test Coupons 20
8.2.1 Evaluation Coupons 20
8.2.2 Test Coupons 20
8.3 Quality Assurance Provisions 20
8.4 Coupons Description 21
8.5 Quantity of Coupons 21
9.0 DELIVERABLES 22
9.1 Preparation for Shipping between Facilities 22
9.2 Lot Deliverables 22

1.0 PURPOSE AND SCOPE

The purpose of this specification is to establish the requirements for the production of Rigid, Rigid-Flex and Flex Printed Wiring Boards that will meet the reliability and performance requirements of Blue Canyon Technologies (BCT). The requirements established in this document apply to the end-product. However, specific process instructions may be outlined where BCT deems it necessary. This specification applies to Rigid, Rigid-Flex and Flex Printed Wiring Boards produced for BCT that reference this specification on their Fabrication/Master Drawings or Purchasing Order.

2.0 REFERENCED STANDARDS AND SPECIFICATIONS

Industrial and Governmental specifications referenced in the document apply only to the extent specified herein. The specifications used in a referenced document apply to the extent specified in the referenced document. Revision letters, when designated, are used. If a revision letter is not shown, the revision in effect at the date of the Request-For-Quote is applicable.

- *IPC-T-50 Terms & Definitions for Interconnecting and Packaging Electronic Circuits*
- *IPC-4562 Metal Foil for Printed Board Applications*
- *IPC-CF-152 Composite Metallic Material Specification for Printed Wiring Boards*
- *IPC-222X Series of Standards on Printed Board Design*
- *IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards*
- *IPC-420X Series of Specifications for Dielectrics Used in Flexible Printed Boards*
- *IPC-601X Series of Qualification and Performance Specifications*
- *IPC-9252 Requirements for Electrical Testing of Unpopulated Printed Boards*
- *J-STD-003 Solderability Tests for Printed Boards*
- *J-STD-004 Requirements for Soldering Fluxes*
- *J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications*
- *IPC-TM-650 2.4.21.1 Bond strength Surface Mount Lands Perpendicular Pull Method*
- *IPC-TM-650 2.6.8 Thermal Stress, Plated-Through Holes*
- *IPC-TM-650 Method 2.4.22 Bow and Twist (Percentage)*
- *MIL–PRF–31032 General Specification for PCB/PWB*

- *MIL–PRF–55110 General Specification for Rigid Printed Wiring Boards*
- *ASTM D 3638-85 Comparative Tracking Index of Electrical Insulating Materials*
- *IEC-112 Comparative Tracking Index of Electrical Insulating Materials*
- *NASA SP-R-0022A Vacuum stability requirements of polymeric material for spacecraft application*
- *ESA ECSS-Q-ST-70-02C Thermal vacuum outgassing test for the screening of space materials*
- *BCT 0PR0187 Printed Wiring Assembly Process Requirements*
- *BCT MP-750 Control of Manufacturing*
- *BCT QP-003 Supplier Quality Requirements*

3.0 TERMS, ACRONYMS AND DEFINITIONS

Reference IPC-T-50 for PWB related terms and acronyms used throughout this document.

LOT: All boards of the same Part Number and Date Code shipped to BCT in one shipment.

FLIGHT, EDU, PROTO, GSE, DEMO: Identifiers of type of the finished product ordered by BCT. The Identifier is stated on Fabrication/Master Drawing, or within PWA/PWB part number description. If not, it should be provided in an email by BCT PCB Manager or by the Responsible Engineer for that board.

CAUTION	*PWB / FPC Manufacturers are to halt processing of BCT order if Board Type Identifier was not supplied by one of the approved methods.*

Unless explicitly noted otherwise on Fabrication/Master Drawing or Purchase Order,

- **FLIGHT** and **EDU** boards are **IPC Class 3 High *Reliability Electronic Products***
- **PROTO**, **GSE** and **DEMO** boards are **IPC Class 2 *Dedicated Service Electronic Products***

4.0 QUALIFICATION

Purchasing and Supplier Quality works with the PCB Manager to identify qualified PWB suppliers. This list is used to inform PWA suppliers of the PWB suppliers BCT has approved, and they are able to purchase

the bare boards from for BCT PWA's. PWB suppliers will only be on the BCT ASL if BCT is buying product directly from the PWB supplier.

4.1 Determination of Manufacture Qualifications

Manufacturers furnishing bare boards products have been determined qualified using the supplier qualification process in QP-540. Qualified board suppliers have demonstrated ability to fabricate products that meet the Qualification Testing requirements as specified in this document.

4.2 Qualification of Special Features

Separate qualifications as specified by BCT Engineering may be required for additional special PWB features like HDI, microvias, constraining/heatsinking cores, embedded passives, book binder stack, etc.

5.0 RESOLUTION OF CONFLICTING REQUIREMENTS

In cases of conflicting requirements, the descending order of precedence for Procurement Documents is:

1. Purchase Order and notes included therein.
2. Fabrication/Master Drawing.
3. This Specification.
4. "Fab Notes" document on legacy designs.
5. BCT Standards and Procedures referenced in this Specification.
6. Industry Standards referenced in this Specification.

CAUTION	*If conflicts found between the Specification, Artwork, or Database, etc. are not addressed, notify BCT immediately for resolution before proceeding with the fabrication of the boards.*

6.0 DEVIATIONS

When the fabrication drawing requires construction to this specification, orders are allowed to deviate from this specification by one of two methods:

- The Fabrication/Master drawing calls out exceptions to the specification by either referencing an alternate specification or a direct statement of the exception requirements.

- Engineering prototype work that requires exceptions that are not noted on the fabrication drawing must be approved in writing by the authorized BCT personnel and the approval documented in the purchase order.

When the finished product deviates or expected to deviate from this specification or deviates from the alternate requirements outlined in the steps listed above, the supplier must follow the appropriate Deviation Waiver Request process for the product to be accepted by BCT.

For clarity of communication, the suppliers are requested to indicate the following codes for deviations within their Request forms:

- **SD1** (Unable to fabricate without Artwork changes) triggers BCT SD NCR process,
- **SD2** (IPC Class downgrade) triggers BCT SD NCR process,
- **SD3** (non-class design deviations/inquiries) EQ/TQ spreadsheet signoff,
- **SD4** (non-class material deviations/inquiries) EQ/TQ spreadsheet signoff,
- **SD5** (Technical Questions, requests to clarify) email response or EQ/TQ spreadsheet signoff.

7.0 PWB/FPC FABRICATION

7.1 Materials

All **FLIGHT** boards materials shall meet outgassing requirements of SP-R-0022A or ECSS-Q-ST-70-02C.

7.1.1 Laminate

Unless explicitly noted otherwise on Fabrication/Master Drawing or Purchase Order,

Rigid Laminate and Multilayer Bonding materials for Rigid **FLIGHT** and **EDU** boards is:
- Glass reinforced polyimide, conforming to *IPC-4101 Specification Sheet 41*.

Rigid Laminate and Multilayer Bonding materials for Rigid **GSE** and **DEMO** boards is:
- Glass reinforced epoxy, conforming to *IPC-4101 Specification Sheet 126*.

Rigid Laminate and Multilayer Bonding materials for Rigid **PROTO** boards is:
- Glass reinforced epoxy, conforming to *IPC-4101 Specification Sheet 126*.

No- or Low- Flow prepregs for all Rigid-Flex boards is:
- Polyimide based, conforming to *IPC-4101 Specification Sheet 42*.
- **Pre-approved: Arlon 37N, Arlon 38N; *GIA-671N is acceptable.**

HDI prepregs:
- Polyimide based boards, **Pre-approved: Arlon 86HP**
- High-Tg FR4 based boards, **Pre-approved: Isola 370HR**

Flex Core:
- adhesive-less polyimide, per *IPC-4204 Specification Sheet 11*

Flex Bondply:
- polyimide w/acrylic adhesive, per *IPC-4203 Specification Sheet 1*

Flex Adhesive:
- acrylic adhesive, per *IPC-4203 Specification Sheet 18*

Flex Coverlay:
- polyimide w/acrylic adhesive, per *IPC-4203 Specification Sheet 1*

Flex shield:
- silver-filled flexible epoxy inks
- **Pre-approved inks: Tatsuta SW180, DuPont (Micromax) CB028**

Laminate materials, unless specified otherwise, shall meet the following requirements:
- Underwriters Laboratory UL94 rating between HB and V0 inclusive
- Minimum Comparative Tracking Index of 175 volts when tested per *ASTM D 3638-85* or *IEC-112*.

Oxide surface treatment is required on inner layers to increase copper surface area and promote lamination bond strength.

Additional Certificate of Conformance is necessary when procuring material with special requirements.

7.1.2 Metallic Foil

Copper Foil for rigid boards in accordance with IPC-4562 type E grade 3.

Copper Foil for flex boards in accordance with IPC-4562 type W grade 7.

Minimum copper foil - Internal	1/4 oz	0.0004in (9 µm)
Maximum copper foil - Internal	3 oz	0.0042in (105 µm)
Minimum copper foil - External	1/4 oz	0.00035in (9 µm)
Maximum copper foil - External	2 oz	0.0028in (70 µm)

7.1.3 Constraining and Heatsinking Cores

Metallic Foils such as Copper or Copper/Invar/Copper (CIC) are per Fabrication/Master Drawing and in conformance with *IPC-4562* for Copper or *IPC-CF-152 for Constraining Composite Core Material*.

- Unless otherwise specified on the Fabrication/Master Drawing, the Constraining Cores material is 0.006in (150 µm) thick with a construction composition ratio of 12.5% / 75% / 12.5%, respectively.
- Unless otherwise specified on the Fabrication/Master Drawing, the Heatsinking Cores material is 4oz/ft^2 Copper Foil.

Qualifications for a Supplier furnishing boards with constraining or heatsinking cores are in addition to the normal Qualification and shall include Vertical and Horizontal Microsections of the clearance holes and the holes connected to the core.

7.1.4 Solder Mask

Solder mask to be applied over bare copper (SMOBC) and shall meet *IPC-SM-840 Class H*.

Solder Mask Thickness range is 0.0002in (5 µm) to 0.0014in (35 µm) when measured over copper plating.

Maximum Solder Mask Thickness is 0.003in (75 µm) when measured over laminate.

Unless indicated otherwise in Fabrication/Master Drawing or Purchase Order Notes, Solder Mask Colors are:

- **GREEN** for **FLIGHT** boards
- **BLUE** for **EDU** boards
- **RED** for **PROTO** boards
- **CLEAR** for **DEMO** boards
- **GREEN** for **GSE** boards

Preferred Solder Mask process is Direct Imaging, either Laser or LED. Solder mask materials that are pre-approved for use are:

- **TAIYO PSR-4000BN DI**
- **TAIYO PSR-4000 DI**
- **TAIYO PSR-4000 LDI**
- **TAIYO PSR-4000 HFX DI**
- **TAIYO PSR-9000 LDI (FOR FPC ONLY)**
- **TAIYO FLEXFINER (FOR FPC ONLY)**

Equivalent masks can be used with BCT approval.

The solder mask application is to cover conductors, areas between Surface Mount component lands; areas between lands and via holes; as well as bare laminate areas and areas adjacent to the lands. Solder mask does not cover lands associated with through-hole components and surface mount lands.

7.1.4.1 Solderable Surface Pattern

The solderable surfaces clearance for SMT lands and through-holes is 0.002in (50 µm) nominal, unless otherwise specified on the Fabrication/Master Drawing or Supplied Artwork.

A modification to the supplied Artwork to achieve the clearance requirement is the responsibility of the Manufacturer.

7.1.4.2 Solder Mask Webbing

Minimum solder mask web width is 0.004in (100 µm). While the requirement is to meet the Master Artwork data provided, it is the responsibility of the Manufacturer to ensure thinner webs of solder mask are removed from the production Artwork.

7.1.4.3 Defect Coverage

Defects are touched up with a material compatible with the applied solder mask or equal to resistance for soldering and cleaning.

7.1.4.4 Registration Errors

Regardless of registration errors, solder mask intrusion onto a land pattern shall not exceed 0.001in (25 µm).

Registration errors allow up to 0.005in (125 µm) of bare areas next to the land.

Blisters bridging conductors are not acceptable.

7.1.4.5 Bare Laminate Areas

As a general guideline, minimize the amount of bare laminate areas.

Bare laminate areas shall not bridge between conductors or between conductors and lands.

Pinholes, voids, skips, and blisters shall not expose conductors or lands in areas where solder is not required.

7.2 PWB/FPC Thickness

Thickness is specified on the Engineering Documentation.

- Board thickness below 0.040in (1mm) has a tolerance of ± 0.005in (125 µm)
- Board thickness between 0.040in (1mm) and 0.085in (2.1mm) has a tolerance of ± 0.008in (200 µm).
- Board thickness over 0.085in (2.1mm) has tolerance of ± 10%

7.3 Dielectric Separation

Dielectric Separation is the minimum measurement between metal peaks or nodules on cladding or plating, as indicated in *IPC-4101, Figure 3-1*.

- Minimum *final* **prepreg** dielectric separation between conductive layers is 0.003in (75 µm).
- Minimum *designed* **rigid core** dielectric separation between conductive layers is 0.003in (75 µm).
- Minimum *designed* **flex core** dielectric separation between conductive layers is 0.001in (25 µm).
- Minimum *final* **flex adhesive** dielectric separation between conductive layers is 0.001in (25 µm).

Dielectric separation on existing products shall not be changed from lot to lot unless such requirement is explicitly noted on Master Drawing or Purchase Order.

7.4 Conductors

- Conductor widths on external or internal layers does not change by more than 20% of the width by any defect such as voids, nicks, undercutting, line width reduction, or roughness.
- Conductor spacing adjustments during fabrication shall not exceed 0.004in (100 µm) or 25% of the indicated spacing on the Fabrication/Master Drawing, Master Pattern or Database, whichever is less.
- Scratches extending more than 0.0002in (5 µm) in depth into the copper surface of external layers are not acceptable.

Minimum **designed** feature width/spacing* and hole to copper spacing* are given in the following table:

Inner Layers	Imperial	Metric
Minimum *designed* copper-to-hole spacing, 1/2-ounce copper or less	0.010”	250 µm
Minimum *designed* copper-to-hole spacing, 1-ounce copper	0.011”	275 µm
Minimum *designed* copper-to-hole spacing, 2-ounce copper	0.012”	300 µm
Minimum *designed* copper-to-hole spacing, 3-ounce copper	0.014”	350 µm
Minimum *designed* hole-to-hole spacing (**without** etchback requirement)	0.013”	325 µm
Minimum *designed* hole-to-hole spacing (**with** etchback requirement)	0.015”	375 µm
**Minimum designed feature width/spacing, 1/4-ounce copper	.0025"/.0025"	62 µm / 62 µm
Minimum *designed* feature width/spacing, 3/8-ounce copper	.003"/.003"	75 µm / 75 µm
Minimum non-plane *designed* feature width/spacing, 1/2-ounce copper	.0035"/.0035"	88 µm / 88 µm
Minimum non-plane *designed* feature width/spacing, 1-ounce copper	.005"/.005"	125 µm / 125 µm
Minimum *designed* feature width/spacing, 2-ounce copper	.008"/.008"	200 µm / 200 µm
Minimum *designed* feature width/spacing, 3-ounce copper	.011"/.011"	275 µm / 275 µm
Add 0.001” (25 µm) for 1/2-ounce & 1-ounce copper planes spacing		
Plated External Layers (with 1 plating cycle)		
**Minimum non-plane *designed* feature width/spacing, 1/4-ounce foil	.003"/.0035"	75 µm / 88 µm
Minimum non-plane *designed* feature width/spacing, 3/8-ounce foil	.004"/.004"	100 µm / 100 µm
Minimum non-plane *designed* feature width/spacing, 1/2-ounce foil	.005"/.005"	125 µm / 125 µm
Minimum non-plane *designed* feature width/spacing, 1-ounce foil	.006"/.006"	150 µm / 150 µm
Minimum non-plane *designed* feature width/spacing, 2-ounce foil	.012"/.012"	300 µm / 300 µm
Add 0.001” (25 µm) for planes spacing		
Plated External Layers (with 2 plating cycles)		
**Minimum non-plane *designed* feature width/spacing, 1/4-ounce foil	.004"/.004"	100 µm / 100 µm
Minimum non-plane *designed* feature width/spacing, 3/8-ounce foil	.005"/.005"	125 µm / 125 µm
Minimum non-plane *designed* feature width/spacing, 1/2-ounce foil	.0055"/.0055"	137 µm / 137 µm
Minimum *designed* feature width/spacing, 1-ounce foil	.007"/.007"	175 µm / 175 µm
Minimum non-plane *designed* feature width/spacing, 2-ounce foil	.012"/.012"	300 µm / 300 µm
Add 0.001” (25 µm) for planes spacing		
Plated External Layers (with 3 plating cycles)		
Minimum non-plane *designed* feature width/spacing, 3/8-ounce foil	.0055"/.0055"	137 µm / 137 µm
Minimum non-plane *designed* feature width/spacing, 1/2-ounce foil	.0065"/.0065"	162 µm / 162 µm
Minimum non-plane *designed* feature width/spacing, 1-ounce foil	.008"/.008"	200 µm / 200 µm
Add 0.001” (25 µm) for planes spacing		

***Spacing is applicable to 0-30 Volt potentials only**
****Optional capability, for example, mSAP applications**

- Absolute minimum **finished** manufactured conductor width is 0.0025in (62 µm).

- Absolute minimum **finished** manufactured conductor spacing is 0.0025in (62 µm).
    - For voltage potentials above 30 Volts, it is the responsibility of BCT Designers to increase spacing numbers in the table above by the difference between the absolute minimum finished manufactured conductor spacing of 0.0025in (62 µm) and the minimum electrical clearance value specified in the Table 6-1 of IPC-2221.
- Minimum **finished** manufactured spacing between unmasked conductive features on surface layers is 0.005in (125 µm)
- Conductor location tolerances are per Producibility Level **C** of *IPC-2221* **or better.**

7.5 Hole Tolerances and Registration

- Holes sizes for lead-in-hole component mounting shall be specified on the Master Drawing as the nominal finished diameters (FHS).
- To convey drilled hole size (DHS), Master Drawing shall use tolerance of +0/- “nominal diameter”.

Hole diameter tolerances, unless stated otherwise on the Master Drawing, given in the following table:

Hole Diameter	Plated Holes Tolerance	Un-plated Holes Tolerance
Vias <0.016in (0.4mm)	+0.003in (75 µm), - “nominal diameter”	N/A
PTH <0.016in (0.4mm)	±0.002in (50 µm)	N/A
≥0.016in (0.4mm) and ≤0.076in (1.93mm)	±0.003in (75 µm)	+0.001in (25 µm), -0.004in (100 µm)
>0.076in (1.93mm) and ≤0.128in (3.25mm)	±0.004in (100 µm)	+0.001in (25 µm), -0.006in (150 µm)
>0.128in (3.25mm) and ≤0.500in (12.7mm)	±0.005in (125 µm)	+0.002in (50 µm), -0.008in (200 µm)

- Specified tolerances shall NOT allow annular ring requirements to be violated.
- The layer-to-layer registration between any two layers shall be controlled to not violate any annular ring requirement for holes.
- Hole positional tolerances are per Producibility Level **C** of *IPC-2221* **or better.**
- Edges of Drilled Holes closer than 0.010in. (250 µm) to each other are **not allowed**.

7.5.1 Annular Ring

Unless indicated otherwise on the Fabrication/Master Drawing, the Annular Rings shall meet the requirements of IPC-6012 standard for the corresponding Class of the board.

7.6 Drilling

The holes in Double Sided boards may use chemical processes for smear removal. Etchback is not required for Double Sided boards.

The holes in multilayer boards must be cleaned using plasma for the lateral removal of material from the internal layers prior to plating.

- After plating, there must be no evidence of resin smear or epoxy residue.
- After plating, there must be a direct bond of the plated copper to foil copper of the internal layer.

7.6.1 Etchback *

Measurement of etchback depth is taken from the edge of the internal copper and the plated barrel in the hole. Etchback requirements defined for **EDU** & **FLIGHT** boards and are as follows:

- Preferred etchback is: 0.0005in (13 µm)
- Minimum etchback is the evidence of positive etchback visible in cross-section.
- Maximum etchback is: 0.0015in (37 µm)
- Wicking may extend an additional **0.002in (50 µm)**, provided it does not reduce the spacing of metallic features below 0.003in (75 µm).
  - *** Note: this requirement exceeds IPC-6012 Class 3**
- Shadowing is allowed on external conductors and on one side of internal lands.
- Negative etchback is not allowed.

Unless stated otherwise in Fabrication/Master Drawing or Purchase Order, etchback requirements are **not** defined for **GSE, PROTO** and **DEMO** boards. Total dielectric removal allowance for **GSE, PROTO** and **DEMO** boards shall be per Class 2 of IPC-6012.

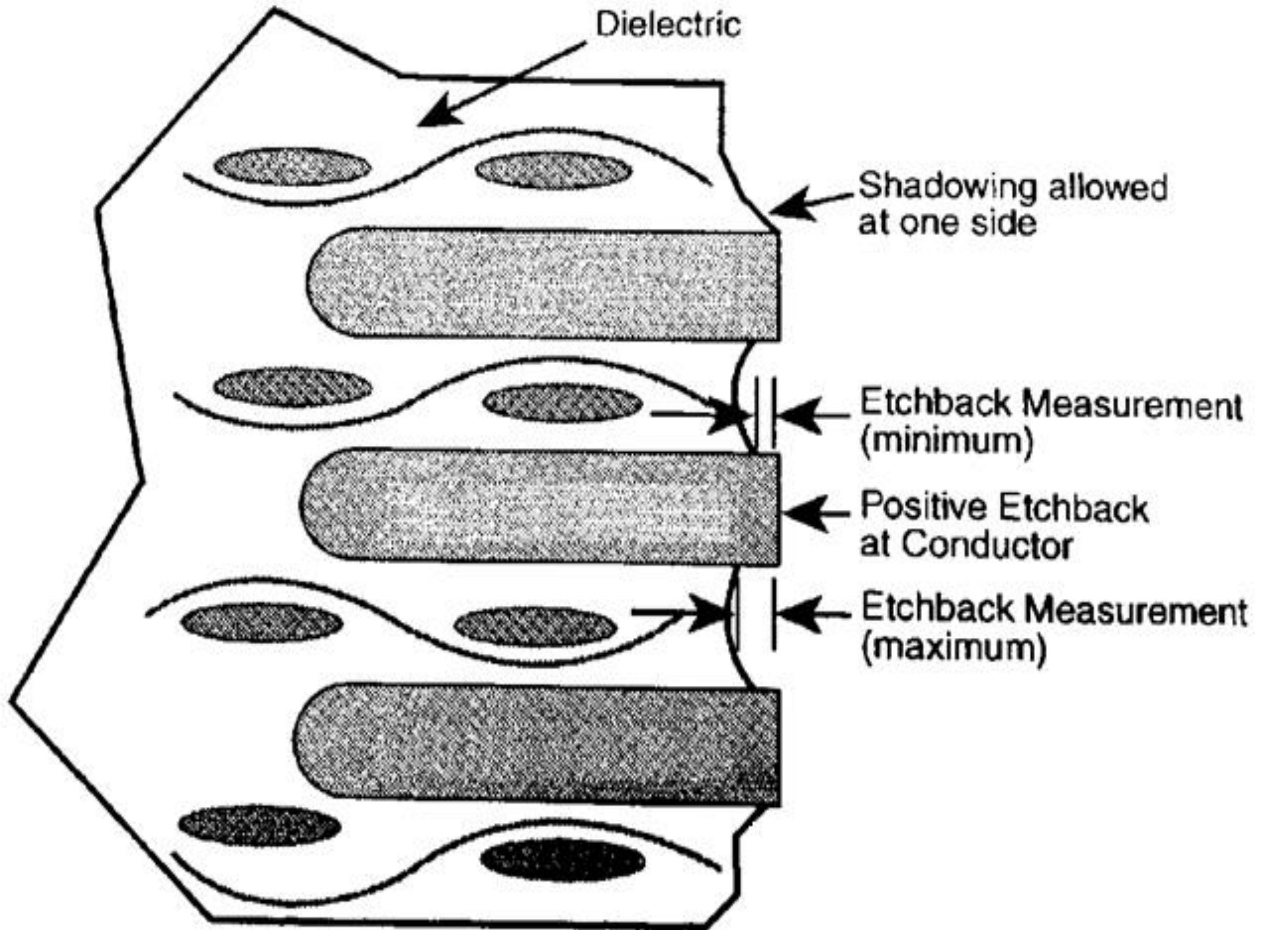

Figure 1 Positive etchback

7.7 Copper Plating

Unless stated otherwise in Fabrication/Master Drawing or Purchase Order:

- copper plating in plated through-holes and via holes, except for buried and blind vias, is 0.001in (25 µm) minimum thickness.
- If buried/blind via hole has a length of no more than 0.007in (180 µm), the minimum copper plating in the buried via holes of internal layers is 0.0007in (18 µm).
- If the buried/blind via hole has a length >0.007in (180 µm), the minimum copper thickness in the hole is 0.001in (25 µm).
- Absolute minimum finished surface conductor thickness for rigid boards (foil + plating) is 0.001in (25 µm).
- Absolute minimum wrap plating is 0.0002in (5 µm).

7.7.1 Copper Voids in Holes

Copper voids are NOT allowed in the holes when viewed visually or in microsection.

7.8 Via Plugging and Capping *

Unless indicated otherwise in Fabrication/Master Drawing, all Vias in rigid stacks shall be protected per IPC-4761 Type VII by filling with nonconductive material and capped by Cu plating.

- Minimum Cu capping thickness is 0.0004in (10 µm)
- Type VII protection is only applicable to drilled Via hole diameters in the range of 0.008in (200 µm) to 0.020in (500 µm).
- Maximum filled and capped via Depression (Dimple) – 0.002in (50 µm)
  - *** Note: this requirement exceeds IPC-6012 Class 3**
- Maximum filled and capped via Protrusion (Bump) – 0.002in (50 µm)

The pre-approved via filling material is San-Ei PHP-900 IR-6P, PHP-900 IR-10[F/FE]

7.9 Rigid-Flex Strain Relief

Tunable flexibility epoxy bead shall be applied to all rigid-flex transitions. Material that is pre-approved for strain relief beads:

- **LOCTITE ABLESTIK 45 with LOCTITE CAT 15**

7.10 HDI (High Density Interconnects)

- Maximum number of lamination cycles for HDI stacks is 4.
- Laser drill diameter is 0.006in (150 µm) for dielectrics up to 0.004in (100 µm) thick.
- Minimum target and capture lands diameter is 0.012in (300 µm)
- All µVias shall be Copper filled.
    - Target copper filled µVia Protrusion/Depression is +/- 0.001in (25 µm), but no less than +/- 0.002in (50 µm).
        - *** Note: this requirement exceeds IPC-6012 Class 3**
- Stacking of µVias (one µVia on top of another µVia) is limited to 2.
- Stacking of µVias on top of mechanically drilled holes is NOT allowed.

7.10.1 Requirements for µVias Target Lands Contact

- If the µVia penetrates the land: the area of interconnection to the terminating land is 100% circumferential.
- If the µVia terminates on the surface of the land: the contact is a “defect free” continuous area that is at least 50% of the capture land area.

7.11 Final External Finishes

The final external finish for the surface and plated through-holes are one of the following as designated on the Fabrication/Master Drawing or Purchase Order. If a final finish is not designated, the default finish is assigned as P-1. Final external finish on existing products shall not be changed from lot to lot unless such requirement is explicitly noted on Fabrication/Master Drawing or Purchase Order.

Plating type P-1 - (**ENIG**) Electroless Nickel/Immersion Gold per the latest revision of IPC-4552. It is selectively applied to the remaining copper exposed after the solder mask has been applied.

Plating type P-2 - (**ENEPIG**) Electroless Nickel/ Electroless Palladium/ Immersion Gold per the latest revision of IPC-4556. It is selectively applied to the remaining copper exposed after the solder mask has been applied.

Plating type P-3 - (**HOR**) Tin-Lead Hot Oil Reflow. The HOR Tin-Lead coating shall be 0.0002 - 0.0005 inch [5 to 12.5 µm] thick prior to fusing/reflow.
For some boards with relaxed requirements, HOR finish may be substituted with HASL (Hot Air Solder Level) with BCT approval.

7.12 Silk Screen

Silk Screen legend is a permanent, epoxy based, non-conductive ink. It is white color unless specified otherwise in documentation provided to the Manufacturer. Silkscreen ink does not cover any exposed solderable surfaces, internal surface of non-plated thru holes, or board edges. The Manufacturer is responsible for clearing portions of silk screen legends provided in the Master Artwork to prevent violations.

Application process is Inkjet, LPI, or another process that ensures 0.004in (100 µm) stroke legibility.

Pre-approved inks are:

- **IJR-4000 FW100**
- **IJR-4000 MW300**
- **PSR-4100 HD**

7.13 Markings

Permanency is described as no loss of legibility exhibited when subjected to soldering and cleaning requirements. Marking is legible, permanent and set in a contrasting color to the base material, white is generally used, unless specified otherwise. Marking ink does not cover any exposed solderable surfaces, internal surface of non-plated thru holes, board edges, or obscure any uncapped via holes. The Manufacturer is responsible for clearing portions of the marking to prevent violations.

- Master Pattern information includes:
  - Company logos
  - Part Numbers and
  - Geometric Shapes

The information is “written” on the conductor pattern using a method which does not degrade the conductor geometry and isolation such as:

- Etch
- Handprint or
- Silk Screen

The Date Code is placed in a location clear of any component(s), using the following methods:

- Stamp
- Handprint
- Silk Screen

7.13.1 Required Markings

- Fab part numbers and revision level designated on the master drawing.
- Component designators and locators provided on the master drawing or artwork.
- Manufacturer's Company logo or company name.
- "Date code" indicating week and year of manufacture and serial numbers corresponding to test coupons.
- Plating Type: P-1, P-2, or P-3 (see *Final External Finishes*).

7.14 Panelization

Soldering techniques and component placement equipment make it desired to add framing material referenced as break-away tabs. Only approved type of break-away for BCT boards is mouse-bite. The mouse-bites shall be placed as far away from ceramic capacitors as practical but no less than 0.125in. If this is not possible, supplier and BCT should consider fully routing the boards and using fixtures to move boards through automation lines and soldering processes. Alternate low impact de-paneling methods like laser singulation may also be considered.

7.15 Repairs

Weld repairs of conductor traces or drilling of internal layer shorts are **not allowed**.

7.16 Electrical Testing

Electrical testing to be performed per IPC-9252 and includes testing of all circuits on all Multilayer Boards for continuity, shorts and isolation resistance. Double-sided boards can be tested by either the same electrical methods or by an Automatic Optical Inspection (AOI).

- Shorts – leakage (unless specified otherwise):
  - Class 3: 50 MΩ at a minimum of 250 Volts
  - Class 2: 10 MΩ at a minimum of 100 Volts
- Opens – continuity (unless specified otherwise):
  - 10 Ω (maximum permitted current thru tested structures is 10 milliamperes)

7.17 Finished Properties

7.17.1 Solderability and Structural Integrity

Solderability of **FLIGHT** and **EDU** products is tested with SnPb solder per *J-STD-003* Category 3/Category B Coating Durability, Class 3. Alternative preconditioning (stressing) for the tests (2x Reflow from IPC-TM-650, 2.6.27) is acceptable.

Before solder testing, all coupons shall be dried for duration of 2 hours at 257°F (125°C).

- **Structural Integrity** testing is performed on Test Coupons A and B per *J-STD-003 Solder Float Test (Chapter 4)*. Evaluate microsections per *IPC-6012 Table 4-3*
- **Hole Solderability** testing is performed on Test Coupon A per *J-STD-003 Solder Float Test (Chapter 4)*. Evaluate per *IPC-6012 Table 4-3*
- **Surface Solderability** testing is performed on Test Coupon M or an equivalent test piece from a production board per *J-STD-003 Edge Dip Test (Chapter 4).* Suppliers without dipping equipment may use tweezers for dipping. Evaluate per *IPC-6012 Table 4-3*

Default testing conditions of the *J-STD-003* shall be modified as follows:

- **Flux type is ROL0/REL0 per *J-STD-004*.**

7.17.2 Edges of the Board

The edges of the board are cleanly routed without excessive roughness or chipping. Maximum delamination, haloing or other edge defects does not extend into the board more than 0.030in (760 µm) or decrease the unaffected distance to any line, pad, or hole by more than 50%, whichever is less.

Edge cracks and chip that span vertically more than two layers thru PWB are not permitted unless reviewed by BCT Quality/Mission Assurance and approved through appropriate NCR Process.

7.17.3 Bow and Twist

Bow & twist shall not exceed 0.75% when measured per *IPC-TM-650 Method 2.4.22.*

8.0 CONFORMANCE AND ACCEPTANCE

8.1 Microsection Evaluations

All Microsection Evaluations are performed after Solder Float Per J-STD-003 4.4.

8.2 Evaluation Coupons and Test Coupons

8.2.1 Evaluation Coupons

Evaluation Coupons is part of every panel used to produce PWB. The Coupons are stored by the Vendor for a minimum period of three years. During the three-year period, Coupons may be requested from the Vendor to be analyzed by BCT. Coupons positioned adjacent to each other as well as adjacent to the marking information specified below:

- Vendor Name or Logo.
- BCT Part Number and Revision letter.
- Date Code and Serial Numbers corresponding to individual boards.
- Plating Type: P-1, P-2, or P-3 (see *Final External Finishes*).
- Coupon Type

Note	Other coupons may be used and positioned at the opposing corners of each panel.

8.2.2 Test Coupons

Test Coupons reflect the specific board characteristics such as, requirements for holes, conductors, and spaces. Test Coupons are used to establish process control parameters consistently used in a single hole size or land configuration which reflects the process.

If provided by BCT Artwork or Design Database does not include required Test Coupons, the Supplier shall add them to the panel in accordance with IPC-2221.

With written approval from BCT, production boards may be used to evaluate and verify conformance to this specification.

8.3 Quality Assurance Provisions

IPC-6012 Table 4-3; *Acceptance Testing and Frequency* are used, unless exceptions, modifications, or additions are noted in the Purchase Order or Fabrication/Master Drawing. Requirements for the inspections are performed by Microsection; Electrical Test; Visual Inspection, or Measurement shown in *IPC-6012; Table 4-3*. The sampling plan in *Table 4-2* and the Test Sample for each Class. The Test Sample is a Board or Test Coupon as designated in the *Table 4-3.* The Test Methods used are referenced as well.

IPC-6012 Table 4-4; *Quality Conformance Testing* is performed unless equivalent testing on similar boards and materials is performed by the Supplier to comply with IPC and retain the qualification to MIL–PRF–31032.

BCT does not require *ED Copper Properties* and *Rework Simulation* tests, but results of the remaining testing shall be provided to BCT upon request.

8.4 Coupons Description

Coupon A and B

In order to inspect the panel for structural integrity, plating thickness, annular ring, etchback, laminate integrity, laminate cracks, copper cracks and other requirements that are specified in *IPC-6012*.

IPC-6012 requires a coupon to be solder floated (thermal stress) and then microsectioned. The microsectioned coupon is either Coupon A or B on each panel.

If metal cores are used in the board, a Horizontal Microsection is made to check for radial cracks for Coupon A or B. If Coupon A is used for Microsection in *7.17.1*, then Coupon B is used for Horizontal Microsection.

In order to test for solderability in the holes, it is necessary to solder float Coupon A and inspect for solderability. Specific coupons are as typically used by the Fabricator to allow for solderability testing of surface layers,

Coupon M (or similar type, as preferred by the Fabricator)

Coupon M is used for solderability testing of surface layers. It may also be used for XRF measurements of gold, palladium and nickel thickness; as well as for testing adhesion of the plating finishes on surface mount lands (IPC-TM-650, Method 2.4.1) or adhesive strength of the copper foil to the substrate (ribbon/tape test).

Coupon D

When printed boards contain microvias, conformance testing shall include IPC-TM-650, Method 2.6.27 on a minimum of one IPC-2221 Coupon D for each µVia structure from each fabrication panel. When a structure includes both microvias and buried vias, Coupon D should include the entire structure. Supplier shall generate IPC-2221 Appendix A coupons for this testing.

8.5 Quantity of Coupons

The board manufacturer must test a certain number of Coupons per *IPC-6012;* The minimum number of coupons is based on a sampling plan as shown in *Table 4-2* and *Table 4-3*. Additional coupons are optional, and the Supplier chooses to retain or discard any.

Note	Other Test Coupons may be required by the Engineering or Product Assurance Departments as a regular or periodic requirement. The requirements shall be specified on the Procurement Documentation or the Fabrication/Master Drawing.

9.0 DELIVERABLES

9.1 Preparation for Shipping between Facilities

Prior to packaging, boards are baked at 115 ± 10°C for 120 minutes. Boards are packaged within one hour after the last baking cycle. A minimum 4mil-thick anti-static zipper type or a heat-sealable bag is used for packing. Each sealed bag contains:

- maximum of 10 boards, immobilized to prevent abrasion during shipment,
- **corrosion/tarnish inhibiting paper interlaid between boards**,
- desiccant pouch,
- humidity indicator.
  - **The indicator shall not touch the desiccant pouch.**
  - **The indicator shall not show a change in color when received at its destination.**

9.2 Lot Deliverables

Deliverables are defined in QP-003 and QP-013 and communicated to the PWB supplier on the purchase order. Unless noted otherwise on Purchase Order or Fabrication/Master Drawing, Coupons and Microsections shall not be shipped but stored by the Manufacturer for the period indicated earlier in this specification.

Note	Alternate or additional deliverables may be specified on the Procurement Documentation or the Fabrication/Master Drawing.